A2

the art. ~~The inventors have provided with this patent application an Information Disclosure Statement listing a number of published papers in the technical field of multi-streaming processors, which together provide additional background and context for the several aspects of the present invention disclosed herein.~~--

Please replace the paragraph beginning on page 3, line 19 with the following paragraph:

A3

-- Pipeline stages take a single clock cycle, so the cycle must be long enough to allow for the slowest operation. The present invention is related to the fact that there are situations in pipelining when instructions cannot be executed. Such events are called hazards in the art. Commonly, there are three types of hazards:--

Please replace the paragraph beginning on page 7, line 27 and continuing to page 8 with the following paragraph to correct text spacing and alignment:

A4

--Fig. 1a is a simplified diagram of a pipeline in a dynamic, multi-streaming (DMS) processor according to an embodiment of the present invention. In this simplified view the pipeline has seven stages, which are fetch, decode, read, dispatch, execute, access and write. These are the same as described in the background section above, except for the separation of read and dispatch in Fig. 1a to illustrate the functions. Dispatch is important in the present invention in that the present invention adds intelligence to Dispatch, improving the performance of the processor. The fetch stage in the pipeline fetches instructions into the pipeline from the multiple streams, and in an embodiment of the present invention is capable of selective fetching.--

Please replace the paragraph beginning on page 8, line 10 with the following paragraph:

A5

-- Although there is no requirement in operating processors that there be instructions at each stage of a pipeline, it is often true that this is the case, and the inventors choose to illustrate each stage as occupied by a single instruction to avoid confusion in description. In many cases there will be a plurality of instructions at various stages, or none at all.--

Please replace the paragraph beginning on page 10, line 7 with the following paragraph:

A6

-- The new technique takes advantage of the fact that, in a DMS processor, as instructions are fetched to the pipeline from individual ones of the streams, there is freedom in choosing a fetching policy or algorithm that will select, on a cycle-by-cycle basis, from which stream instructions are to be fetched.--

Please replace the paragraph beginning on page 13, line 11 with the following paragraph:

A7

-- Policy (a) provides the lowest performance since the consumer instruction might be unnecessarily stalled before it is dispatched. The ~~producer~~ consumer instruction will be dispatched as soon as the producer hits in the data cache or, in case it misses, when the missing data arrives from the next level of memory hierarchy. On the other hand, this policy provides the simplest implementation, since no re-scheduling will occur.--

Please replace the paragraph beginning on page 14, line 9 with the following paragraph:

A8

-- The benefits of a hit/miss predictor for dispatch logic are not restricted to multistreaming processors only, but in a multistreaming processor where the technique has larger benefits than in a conventional (single-streaming) processor